REMARKS

Prior to the present amendment and response, claims 93-101, 104-113, and 116-119 were pending in the present application. Claims 93-101, 104-113, and 116-119 remain in the present application and claims 118 and 119 have been allowed. Reconsideration and allowance of outstanding claims 93-101, 104-113, and 116-117 in view of the following remarks are requested.

A. Rejections of Claims 93-99, 104-109, and 116-117 under 35 USC §103(a)

The Examiner has rejected claims 93-99, 104-109, and 116-117 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,792,706 to Michael, et al. (hereinafter "Michael") in view of U.S. patent number 6,040,248 to Chen, et al. (hereinafter "Chen") and U.S. patent number 6,017,814 to Grill, et al. (hereinafter "Grill"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by independent claims 93 and 105, is patentably distinguishable over Michael, Chen, and Grill, singly or in any combination thereof.

The present invention, as defined by independent claims 93 and 105, recites, among other things, forming a first air gap, a second air gap, and a support pillar in a first hard mask and a first insulating layer, and depositing a sealing layer over the first hard mask, where the first insulating layer and the sealing layer comprise a same low dielectric constant material. As disclosed in the present application, a first insulating layer (e.g.

dielectric layer 18) and a sealing layer (e.g. sealing layer 26) can each comprise a low dielectric constant material. Page 8, lines 24-26, and page 11, lines 25-27 of the present application. Since the first insulating layer is situated between first and second interconnect lines and the sealing layer is situated over the first and second interconnect lines, by utilizing a low dielectric constant material to form the first insulating layer and the sealing layer, the present invention can advantageously achieve an interconnect structure having reduced intra-layer capacitance and reduced inter-layer capacitance.

Additionally, as disclosed in reference to one embodiment in the present application, by forming the sealing layer (e.g. sealing layer 26) and the first insulating layer (e.g. dielectric layer 18) from the same material, the present invention advantageously avoids the need to change the etch chemistry when etching a via hole in the sealing layer and the first insulating layer. Thus, by forming a sealing layer and a first insulating layer of the same low dielectric constant material, the present invention advantageously achieves an interconnect structure having reduced intra-layer and inter-layer capacitance and an interconnect structure that can be fabricated with a reduced number of process steps.

In contrast to the present invention as defined by independent claims 93 and 105, Michael does not teach, disclose, or suggest forming a first air gap, a second air gap, and a support pillar in a first hard mask and a first insulating layer, and depositing a sealing layer over the first hard mask, where the first insulating layer and the sealing layer comprise a same low dielectric constant material. Michael specifically discloses forming

first dielectric 20 over and between adjacent lines 11, where first dielectric 20 is preferably formed with a TEOS (Tetra-Ethyl-Ortho-Silicate) source (i.e. a TEOS based oxide). See, for example, column 5, lines 51-55 and Figure 3 of Michael. Michael further discloses that the use of a TEOS source for first dielectric 20 is preferable because it is believed to result in improved step coverage and conformality. See, for example, Michael, column 5, lines 56-59. Michael further states that TEOS based oxides are better able to fill spaces between adjacent lines 11 than silane based oxides, since silane based oxides tend to leave voids when used to fill spaces having aspect ratios greater than 0.5. See, for example, Michael, column 5, lines 59-62.

Thus, Michael clearly states a difference between TEOS based oxides and silane based oxides and why TEOS based oxides are preferably used for first dielectric 20. In Michael, capping dielectric layer 30 is formed on first dielectric 20 to provide a cap for trenches 26 such that subsequent deposition of an interconnect will not produce interconnect material in trenches 26. See, for example, column 6, lines 57-67, column 7, lines 1-2, and Figure 8 of Michael. In Michael, capping dielectric layer 30 preferably comprises a layer of silicon dioxide formed from a silane source. See, for example, Michael, column 6, lines 58-61. Thus, in Michael, a TEOS based oxide is used for first dielectric 20 because of its ability to fill spaces between adjacent lines, while a silane based oxide is used for capping dielectric layer 30 to avoid producing interconnect material in trenches 26.

Thus, in Michael, different dielectric material properties are require first dielectric 20 and capping dielectric layer 30. As such, Michael teaches away from using the same dielectric material for first dielectric 20 and capping dielectric layer 30. Furthermore, Michael fails to teach, disclose, or remotely suggest a first insulating layer and a sealing layer that comprise the same low dielectric constant material, as specified in independent claims 93 and 105. In fact, Michael fails to teach, disclose, or suggest using a low dielectric constant material to form a first insulating layer and a sealing layer.

On page 9 of the Final Rejection dated July 7, 2005, the Examiner states that "TEOS is tetraethoxy silane, thus a TEOS based oxide is a silane based oxide." Applicant respectfully disagrees and submits that TEOS is tetra-ethyl-ortho-silicate, which is not a silane base oxide. Also, on page 9 of the Final Rejection dated July 7, 2005, the Examiner states that Michael discloses that "a TEOS based oxide may be formed as part of the capping layer for an improved planarization layer, thus teaching the use of the same material for the first insulating layer and the capping layer." However, Michael states that "[a]alternatively, in another embodiment not shown, planarization could be preceded by the deposition of an additional dielectric layer, preferably a CVD oxide formed from a TEOS or ozone (O_3) source." Michael, column 7, lines 13-16 (emphasis added). Thus, Michael discloses using an additional TEOS oxide layer over capping dielectric layer 30 (which preferably comprises a silane based oxide) to achieve a more planar upper surface. Thus, Michael clearly does not require that first dielectric 20 and capping dielectric layer

30 comprise the same low dielectric constant material, as specified in independent claims 93 and 105.

In contrast to the present invention as defined by independent claims 93 and 105, Chen does not teach, disclose, or suggest forming a first air gap, a second air gap, and a support pillar in a first hard mask and a first insulating layer, and depositing a sealing layer over the first hard mask, where the first insulating layer and the sealing layer comprise a same low dielectric constant material. Chen is directed to a process for plasma etching of contact and via openings in low-k organic polymer dielectric layers. See, for example, the Abstract of Chen. Chen states that in an effort to improve performance of integrated circuits, various organic insulators such as parylene, and arylene ether polymers have been successfully used as low-k replacements for silicon oxide. See, for example, Chen, column 1, lines 33-40. However, Chen fails to teach, disclose, or remotely suggest a first insulating layer and a sealing layer comprising the same low dielectric constant material, as specified in amended independent claims 93 and 105.

Furthermore, Chen does not teach, disclose, or suggest using a low-k dielectric for improved step coverage and conformality and/or to produce cusping that serves to seal off upper portion of trenches without filling the trenches with the dielectric material. Thus, Chen does not teach, disclose, or suggest a low-k dielectric that can provide the particular benefits (as discussed above) that TEOS oxide and silane based oxide provide in Michael. As such, Chen fails to cure the basic deficiencies of Michael discussed above. Moreover,

Applicant respectfully submits that the Examiner has provided insufficient motivation in the art for the suggested combination of Michael and Chen.

In contrast to the present invention as defined by independent claims 93 and 105, Grill does not teach, disclose, or suggest forming a first air gap, a second air gap, and a support pillar in a first hard mask and a first insulating layer, and depositing a sealing layer over the first hard mask, where the first insulating layer and the sealing layer comprise a same low dielectric constant material. Grill specifically discloses a layer containing metal wiring 7, patterned dielectric 4, and air gaps 5, in which the dielectric patterns have been personalized. See, for example, column 3, lines 15-17 and Figure 5 of Grill. However, Grill fails to teach, disclose, or remotely suggest a first insulating layer and a sealing layer that comprise the same low dielectric constant material, as specified in independent claims 93 and 105. Thus, the combination of Chen and Grill fails to overcome the basic deficiencies of Michael discussed above. Thus, Applicant respectfully submits that the combination of Michael, Chen, and Grill suggested by the Examiner does not and cannot result in the claimed invention.

For all the foregoing reasons, Applicant respectfully submits that the present invention, as defined by independent claims 93 and 105, is not suggested, disclosed, or taught by Micheal, Chen, and Grill, singly or in any combination thereof. Thus, independent claims 93 and 105 are patentably distinguishable over Micheal, Chen, and Grill and, as such, claims 94-101 and 104 depending from independent claim 93 and claims 106-113 and 116-117 depending from independent claim 105 are, *a fortiori*, also

patentably distinguishable over Micheal, Chen, and Grill for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by independent claims 93 and 105, and the claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, dependent claims 94-101, 104, 106-113, and 116-117 are also patentably distinguishable over the art cited by the Examiner. For all the foregoing reasons, an early allowance of outstanding claims 93-101, 104-113, and 116-117 and an early Notice of Allowance for all pending claims 93-101, 104-113, and 116-119 is respectfully requested.

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Respectfully Submitted,
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